REMARKS

In response to the above-identified Office Action, Applicants seek reconsideration thereof. In this response, Applicants do not amend, cancel or add any new claims. Accordingly, Claims 1-9 are pending.

I. Claims Rejected Under 35 U.S.C. §102(a)

The Examiner rejects Claims 1, 3 and 5 under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,111,881 issued to Soncodi ("Soncodi"). Applicants respectfully traverse the rejection.

To anticipate a claim, the relied upon reference must disclose each element of the claim. Among other limitations, independent Claim 1 defines a method comprising mapping a first physical identifier for a first physical signal line to the logical identifier, and remapping a second physical identifier for a second physical signal line to the logical identifier responsive to a line failure on the first physical signal line.

In making the rejection, the Examiner characterizes Soncodi as showing a method including fixing a logical identifier for a signal line at an egress interface; mapping a first physical identifier for a first physical signal line to the logical identifier; and remapping a second physical identifier for a second physical signal line to the logical identifier responsive to a line failure on the first physical signal line. However, Soncodi, at a minimum, fails to teach at least remapping a second physical identifier for a second physical signal line to the logical identifier responsive to a line failure on the first physical signal line as recited in claim 1.

Soncodi teaches a method for rerouting ATM connections within a private network node interface or private network-to-network interface (PNNI) domain. See Soncodi, col. 1, lines 6-10. Soncodi's method "includes the step of determining a new call path connecting a new set of nodes in a peer group and establishing the new call path via the new set of nodes." Soncodi, col. 2, lines 21-24. Referring to Figure 4, Applicants respectfully submit that Soncodi teaches that when a faulty line occurs, a new call path is established. The original call path (C20, C30, C50) is discarded and a new call path (C 20, C40, C50) is established, bypassing node C30. Thus, a second

physical identifier for a second physical signal line cannot be remapped to the logical identifier responsive to a line failure on the first physical line since a new path using a new node is created.

By contrast, in Applicants' claimed method, when a failure is detected on a working signal line, the system switches signals to protection lines within the same node. The signals do not necessarily remain on the protection line until the signals reach their destination. Rather, after a signal is switched to a protection line, the system routes the signal back to its intended working line path at a location past the site of the working lines failure using the same set of nodes. Therefore, the signal arrives at its destination on the working line it was originally intended to arrive on and does not require any additional nodes be included within the system. Thus, Soncodi fails to teach at least these elements of claim 1.

The failure of Soncodi to teach each of the elements of claim 1 is fatal to the anticipation rejection. Therefore, claim 1 is not anticipated by Soncodi. Accordingly, Applicants respectfully request withdrawal of the rejection of claim 1.

Claims 3 and 5 each depend from claim 1 and include each of the elements thereof. Therefore, claims 3 and 5 are not anticipated by Soncodi at least for the same reasons as claim 1. Accordingly, Applicants respectfully request withdrawal of the rejection of claims 3 and 5.

II. Claims Rejected Under 35 U.S.C. §103(a)

A. Soncodi in View of Koenig

The Examiner rejects claims 2 and 4 under 35 U.S.C. § 103(a) as being obvious over Soncodi in view of U.S. Patent No. 6,351,452 issued to Koenig et al. ("Koenig"). Applicants respectfully traverse the rejection.

To render a claim obvious, the relied upon references must teach or suggest each of the elements of the claim. Claims 2 and 4 depend from claim 1 and include all of the elements thereof. Therefore, the discussion above regarding Soncodi failing to teach or suggest each of the elements of independent claim 1 is equally applicable to claims 2 and 4. Thus, Soncodi fails to teach or suggest the elements of at least remapping a second physical identifier for a second physical signal

line to a logical identifier responsive to a line failure on the first physical signal line as recited in claims 2 and 4.

The Examiner relies on Koenig to cure the defects of Soncodi. Applicants respectfully submit Koenig fails to cure the defects of Soncodi.

In making the rejection, the Examiner characterizes Koenig as showing "rewriting the cross connect table and preventing change to the identifier after initialization." See Paper No. 10, page 4 (citing Koenig, Figure 8, col. 5, lines 13-24 and col. 14, lines 9-48). The Examiner does not cite Koenig as teaching or suggesting remapping a second physical identifier for a second physical signal line to the logical identifier responsive to a line failure on the first physical signal line. In addition, in reviewing Koenig in its entirety, Applicants have been unable to discern any sections of Koenig that teach or suggest at least these elements. Therefore, Koenig fails to cure the defects of Soncodi.

The failure of the combination of Soncodi and Koenig to teach or suggest each of the elements of claims 2 and 4 is fatal to the obviousness rejection. Therefore, claims 2 and 4 are not obvious over Soncodi in view of Koenig. Accordingly, Applicants respectfully request withdrawal of the rejection of claims 2 and 4.

B. Byers in View of Reveles

The Examiner rejects claims 6-9 under 35 U.S.C. § 103(a) as being obvious over U.S. Patent No. 5,959,996 issued to Byers ("Byers") in view of U.S. Patent No. 6,075,785 issued to Reveles et al. ("Reveles"). Applicants respectfully traverse the rejection.

To render a claim obvious, the cited references must teach or suggest each of the elements of the claim. Among other elements, claim 6 defines an apparatus comprising a translation module to translate an incoming signal identifier to one of a logical identifier independent of a physical line on which a signal is received. Applicants respectfully submit the combination Byers and Reveles fails to teach or suggest at least these elements of claim 6.

In making the rejection, the Examiner characterizes Byers as teaching a bus interface, an ingress time slot interchange (ITSI) module, a switch fabric coupled to the ITSI module, and an egress time slot interchange (ETSI) module having a plurality of inputs, each input assigned a logical identifier which remains fixed after initialization. See Paper No. 10, page 3. The Examiner admits Byers "does not disclose a translation module to translate an incoming signal identifier to one of the logical identifiers independent of a physical line on which the signal is received." Paper No. 10, page 4. Applicants have reviewed Byers in its entirety and respectfully submit Byers does not teach or suggest a translation module as defined in claim 6. Therefore, Byers fails to teach or suggest each of the elements of claim 6. The Examiner relies on Reveles to cure the defects of Byers, but Applicants respectfully submits Reveles fails to cure the defects of Byers.

The Examiner characterizes Reveles as disclosing "a translation module to translate an incoming signal identifier to one of the logical identifiers independent of a physical line on which the signal is received (See Fig. 3, Abstract, col. 3, lines 19-58)." Paper No. 10, page 4. Applicants have reviewed the sections of Reveles cited by the Examiner and respectfully disagree with the Examiner's characterization of Reveles.

Reveles teaches a method and apparatus for providing a selectable speed data link in a telecommunication system. See Reveles, col. 1, lines 8-10. To provide a selectable speed, Reveles teaches "mapping information as physically stored in the TSSR 260 in groups of 16 which correspond to the N PHDB ports, which in the preferred embodiment N=16." Reveles, col. 3, lines 25-27. In addition, Reveles shows:

> Using the translation for N=16 embodiment described above and shown in Figure 3, linear access to TSSR memory (e.g., 0, 1, 2, 3,) by the control processor 240 results in every 16th location being accessed (i.e., 0, 16, 32, 48). This is in contrast to the linear access of TSSR memory (e.g., 0, 1, 2, 3,) by the timing controller 250 in conjunction with a transmit TSI request response by TSRCTL 264 to change the state of multiplexer 258 which results in sequential TSSR memory locations (0, 1, 2, and 3) being accessed. Col. 3, lines 50-58.

Applicants respectfully submit that Reveles fails to teach a translation module to translate an incoming signal identifier to one of the logical identifiers independent of a physical line on which

the signal is received since Reveles describes the purpose of mapping is to coordinate access to TSSR memory locations in sequential order. By contrast, an apparatus as defined in claim 6 utilizes a translation module to remap a signal from a physical signal line to a protection signal line then back to the physical signal line in response to a line failure in the physical signal line. Therefore, Reveles fails to cure the defects of Byers.

In addition, Applicants respectfully submit that the proper motivation to combine Byers and Reveles does not exist. MPEP § 2143 states, "there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, ...to combine reference teachings." The Examiner claims the motivation to combine Byers and Reveles is "to map and to locate the proper location for each incoming data from the congestion." Paper No. 10, page 4. Applicants respectfully submit that to map and to locate the proper location for each incoming data from the congestion is not a proper motivation since claim 6 is drawn to an apparatus for remapping a signal to a protection line to transmit a signal around a faulty signal line and locating the proper location for each incoming signal to avoid congestion is not relevant to the claimed elements.

The failure of the combination of Byers and Reveles to teach or suggest each of the elements of claim 6 is fatal to the obviousness rejection. Therefore, claim 6 is not obvious over Byers in view of Reveles. Accordingly, Applicants respectfully request withdrawal of the rejection of claim 6.

Claims 7-9 each depend from claim 6 and contain all the elements thereof. Therefore, the discussion above regarding the failure of the combination of Byers and Reveles to teach or suggest each of the elements of claim 6 is equally applicable to claims 7-9. Accordingly, Applicants respectfully request withdrawal of the rejection of claims 7-9.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending (1) are in proper form, (2) are neither obvious nor anticipated by the relied upon art of record, and (3) are in condition for allowance. A Notice of Allowance is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

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Dated: 2/25, 2004

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CERTIFICATE OF MAILING:

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop Non-Fee Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on 2/25/04.

Nadya Gordon 2/25/04

Nadya Gordon Date